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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application No.	10/038,162
Filing Date	January 2, 2002
First Named Inventor	Doron Orenstien
Art Unit	2863
Examiner Name	Tung S. Lau
Total Number of Pages in This Submission	20
Attorney Docket Number	42390P10918

ENCLOSURES *(check all that apply)*

- ☒ Fee Transmittal Form
  - ☒ Fee Attached
- ☐ Amendment / Response
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
  - ☐ PTO/SB/08
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Basic Filing Fee
  - ☐ Declaration/POA
- ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s)
- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☒ Appeal Communication to Group **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) *(please identify below):*

Return receipt postcard

Remarks

Appeal Brief filed in triplicate

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Walter T. Kim, Reg. No. 42,731 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	Walter T. Kim
Date	March 3, 2004

CERTIFICATE OF MAILING/TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Typed or printed name	Marilyn Bass		
Signature	Marilyn Bass	Date	03 - 03 - 04

FEE TRANSMITTAL for FY 2004

Effective 01/01/2004. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT ($) 330.00

Complete if Known	
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METHOD OF PAYMENT *(check all that apply)*

☒ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☐ Deposit Account

Deposit Account Number: 02-2666

Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

The Commissioner is authorized to: *(check all that apply)*

☐ Charge fee(s) indicated below ☒ Credit any overpayments

☒ Charge any additional fee(s) or underpayment of fees as required under 37 CFR §§ 1.16, 1.17, 1.18 and 1.20.

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES

	Extra Claims		Fee from below		Fee Paid
Total Claims		- 25** =		X =	
Independent Claims		- 4 =		X =	
Multiple Dependent				=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple Dependent claim, if not paid
1204	86	2204	43	**Reissue independent claims over original patent
1205	18	2205	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

***or number previously paid, if greater, For Reissues, see below*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920 *	1804	920 *	Requesting publication of SIR prior to Examiner action	
1805	1,840 *	1805	1,840 *	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	1,210	2255	605	Extension for reply within fifth month	
1404	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	330.00
1403	290	2403	145	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	1809	385	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR § 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 330.00

SUBMITTED BY

Complete (if applicable)

Name (Print/Type)	Walter T. Kim	Registration No. (Attorney/Agent)	42,731	Telephone	(310) 207-3800
Signature	Walter T. Kim			Date	03-3-04

Based on PTO/SB/17 (10-03) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 02/10/2004.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Attorney Docket No. 42P10918

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the Patent Application of:

Doron Orenstien, et al.

Serial No. 10/038,162

Filed: January 2, 2002

For: **DETERMINISTIC POWER-ESTIMATION FOR THERMAL CONTROL**

Examiner: Lau, Tung S.

Art Unit: 2863

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P. O. 1450
Alexandria, VA 22313-1450

Dear Commissioner:

Applicant submits, in triplicate, the following Appeal Brief pursuant to 37 C.F.R. § 1.192 for consideration by the Board of Patent Appeals and Interferences. Applicant also submits herewith a check in the amount of $330.00 to cover the cost of filing the opening brief as required by 37 C.F.R. § 1.17(c). Please charge any additional amount due or credit any overpayment to deposit Account No. 02-2666.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

Doron Orenstien and Ronny Ronen, the parties named in the caption, assigned their rights to that disclosed in the subject application through an assignment recorded on January 2,2002 (012449/0210) to Intel Corporation, of Santa Clara, California. Thus, as the owner at the time the brief is being filed, Intel Corporation, of Santa Clara, California is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences that will directly affect or be directly affected by or having a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-27 are pending in the application. The Examiner has rejected all pending claims. Applicant hereby appeals the rejection of all the pending claims.

IV. STATUS OF AMENDMENTS

No amendment has been filed subsequent to the Response to Final Office Action having a mailing date of January 16, 2004.

V. SUMMARY

A system and a related method are disclosed to control the amount of heat generated by microprocessors. (Specification, paragraph 8, lines 1-8). The system includes one or more throttling mechanisms incorporated within a microprocessor and a thermal control subsystem coupled to control activation and deactivation of the throttling mechanism based on an estimated power usage. (Specification, paragraph 8, lines 1-8). The thermal control subsystem includes a power usage monitoring unit to estimate an amount of power consumed by a microprocessor during a given time interval based on the number of occurrences of various activities performed in the microprocessor. (Specification, paragraph 13, lines 1-6). Based on the estimated power usage provided by the power usage monitoring unit, a throttle control unit of the thermal control subsystem generates and sends signals to selectively activate and deactivate the one or more of the throttling mechanisms in order to control the amount of heat generated by the microprocessor. (Specification, paragraph 13, lines 6-10). In accordance with one embodiment,

the power usage monitoring unit communicates with at least one counter incorporated within the microprocessor and estimates the amount of power used by the microprocessor based on information provided by the at least one counter. (Specification, paragraph 14, lines 1-8).

VI. ISSUES

The issue involved in this appeal is as follows:

Under 35 U.S.C. § 102(e), are Claims 1-27 anticipated by Grochowski (U.S. Patent No. 6,564,328)?

VII. GROUPING OF CLAIMS

Applicant contends that the claims can be divided into the following groups and that each group of claims is separately patentable. These groups are as follows:

Group I - Claims 1, 2, 6, 15;

Group II - Claim 3, 16;

Group III - Claim 8, 9, 10, 13;

Group IV Claims 19, 20, 21, 24, 26, 27;

Group V - Claim 4, 11, 17, 22;

Group VI - Claim 5, 12, 18, 23; and

Group VII - Claim 7, 14, 25.

Each claim group is deemed separately patentable for the reasons given below.

Claims 1 and 15 of Group I contain the limitations that an amount of power used by a microprocessor is estimated based on information provided by at least one counter. Since Claims 1 and 15 of Group I contain distinguishable limitations from the cited references, Claims 1 and 15 of Group I is separately patentable. Since Claims 2 and 6 depend on Claim 1, Claims 1, 2, 6 and 15 stand or fall together.

Claims 3 and 16 of Group II contain the limitations that an amount of power used by a microprocessor is on (1) the count value associated with said at least one activity, (2) current clock frequency and (3) operating voltage level of the microprocessor. Since Claims 3 and 16 of Group II contain distinguishable limitations from the claims of other groups and also from the cited references, Claim 3 and 16 of Group II are separately patentable.

Claim 8 of Group III recites a method comprising receiving information provided by at least one counter; estimating an amount of power used by a microprocessor based on the information provided by the at least one counter; and controlling at least one throttling mechanism incorporated in the microprocessor based on said estimated power usage. Since Claim 8 of Group III contains distinguishable limitations from the cited references, Claim 8 of Group III is separately patentable. Since Claims 9, 10 and 13 depend on Claim 8, Claims 8, 9, 10 and 13 stand or fall together.

Claim 19 of Group IV recites machine-readable medium that provides instructions, which when executed by a microprocessor cause said microprocessor to perform operations comprising: [1] receiving information provided by at least one counter; [2] estimating an amount of power used by a microprocessor based on the information provided by the at least one counter; and [3] controlling at least one throttling mechanism incorporated in the microprocessor based on said estimated power usage. Since Claim 19 of Group IV contains distinguishable limitations from the cited references, Claim 19 of Group IV is separately patentable. Since Claims 20, 21, 24, 26 and 27 depend on Claim 19, Claims 19, 20, 21, 24, 26 and 27 stand or fall together.

Claims 4, 11, 17 and 22 of Group V contain the limitations that a current estimated power usage value is averaged with a defined number of most recently estimated power usage values obtained during previous sampling time periods. Since Claims 4, 11, 17 and 22 of Group V contain distinguishable limitations from the claims of other groups and also from the cited references, Claim 4, 11, 17 and 22 of Group V are separately patentable.

Claims 5, 12, 18 and 23 of Group VI contain the limitations that a throttling control unit (or a method) compares the estimated amount of power used by the microprocessor against a threshold and activates the throttling mechanism if the estimated power used by the microprocessor is greater than said threshold or deactivates the throttling mechanism if the estimated power used by the microprocessor is less than said threshold. Since Claims 5, 12, 18 and 23 of Group VI contain distinguishable limitations from the claims of other groups and also from the cited references, Claims 5, 12, 18 and 23 of Group VI are separately patentable.

Claims 7, 14 and 25 of Group VII contain the limitations that at least one of the activities monitored is one of the following activities; (1) floating point operation, (2) cache memory access and (3) instruction decoding. Since Claims 7, 14 and 25 of Group VII contain

distinguishable limitations from the claims of other groups and also from the cited references, Claims 7, 14 and 25 of Group VII are separately patentable.

VIII. ARGUMENT

A. Overview of the Cited References

1. Overview of Grochowski

Grochowski describes a microprocessor with a digital power throttle that estimates a power consumption of the processor based on activity states of the processor's functional units. (Grochowski, column 2, lines 21-26). Specifically, the digital throttle of Grochowski estimates the power consumed by the processor by summing a power weight associated with each functional unit that is currently "on". (Grochowski, column 3, lines 7-21). This is accomplished using a monitor circuit 320 shown figure 3 of Grochowski, which serves to estimate an amount of power consumed by the processor by summing a power weight associated with each functional unit that is currently "on". (Grochowski, figure 3, column 5, line 38 to column 6, line 33). The "accumulated power" computed by the monitor circuit 320 of Grochowski is provided to a throttle circuit 330, which uses the "accumulated power" value to control the flow of instructions through pipeline 120. (Grochowski, figure 3, column 5, line 38 to column 6, line 33). Absent from Grochowski is any teaching or suggestion of estimating an amount of power used by the microprocessor based on information provided by a counter. Furthermore, absent from Grochowski is any teaching or suggestion of controlling a throttling mechanism based on the estimated power usage.

B. Group I: Rejection of Claims 1, 2, 6 and 15 Under 35 U.S.C. §102(e) as Being Anticipated by Grochowski

The Examiner rejects Claims 1, 2, 6 and 15 under 35 U.S.C. §102(e) as being anticipated by Grochowski.

To anticipate a claim, every element of the claim must be disclosed within a single reference. Thus, if even one feature of Claim 1 is not found in Grochowski, Applicant respectfully requests that the rejection of Claim 1 under 35 U.S.C. § 102 must be overturned.

Claim 1 recites a microprocessor comprising: a throttling mechanism; and a thermal control subsystem to estimate an amount of power used by the microprocessor and to control the

throttling mechanism based on the estimated power usage. The claimed thermal control subsystem is in communication with at least one counter and estimates the amount of power used by the microprocessor based on information provided by the at least one counter.

Applicant finds no teaching or suggestion in Grochowski of estimating an amount of power used by a microprocessor based on information provided by at least one counter as claimed by Applicant.

Applicant respectfully submits that Grochowski does not teach or suggest a thermal control subsystem that "estimates the amount of power used by the microprocessor based on information provided by the at least one counter", as recited in Claim 1. Instead , Grochowski teaches a digital throttle that estimates a power consumption of a processor based on activity states of the processor's functional units. Specifically, the digital throttle of Grochowski estimates the power consumed by the processor by summing a power weight associated with each functional unit that is currently "on" (see column 3, lines 7-21 of Grochowski). As seen by referring to Figure 3 and corresponding description in Grochowski, the monitor circuit 320 serves to estimate an amount of power consumed by the processor by summing a power weight associated with each functional unit that is currently "on". Specifically, the monitor circuit 320 of Grochowski includes weight units 314 that provide power level to adder 324 when the activity state signal from its gate unit 310 is asserted and the adder 324 sums the power weights indicated by weights units and substrates the threshold level from the sum. The "accumulated power" computed by the monitor circuit 320 of Grochowski is provided to a throttle circuit 330, which uses the "accumulated power" value to control the flow of instructions through pipeline 120. Importantly, Applicant submits that the throttle circuit 330 shown in Figures 3 and 4 of Grochowski has nothing do with estimating an amount of power used by a processor. Instead, the estimating of an amount of power used by the processor in Grochowski is accomplished in the monitor circuit 320.

In rejecting Claim 1, the Examiner asserts that the limitation that "the thermal control subsystem estimates the amount of power used by the microprocessor based on information provided by the at least one counter" is taught by Grochowski, citing Figure 4, unit 420, column 6-7, lines 66-8 of Grochowski. However, Applicant respectfully submits that the counter 420 (referred in the specification as counter "430") shown in Figure 4 of Grochowski has nothing do with estimating an amount of power used by the processor. Rather, the counter 420 shown in

Figure 4 of Grochowski is used to increment a column index in control unit 420 from 0-127 (see column 7, lines 10-13 of Grochowski). There is nothing in Grochowski that teaches or suggests that the information provided by the counter 420 is used to estimate an amount of power used by the processor, as required by Claim 1. As noted above, the estimation of the power used by the processor, in Grochowski, is accomplished by the monitor circuit 320, shown in Figure 3. In view of the foregoing, Applicant respectfully submits that Grochowski fails to teach or suggest a thermal control subsystem that "estimates the amount of power used by the microprocessor based on information provided by the at least one counter", as recited in Claim 1.

Since Grochowski does not disclose a thermal control subsystem estimating an amount of power used by a microprocessor based on information provided by a counter as recited in Claim 1, the rejection of Claim 1 under 35 U.S.C. §102 as being anticipated by Grochowski is in error.

Analogous arguments and discussion apply to independent Claim 15. Specifically, with respect to independent Claim 15, Applicant respectfully submits that Grochowski fails to teach or suggest a power usage estimator to estimate an amount of power used by a microprocessor based on information provided by at least one counter, as recited by Applicant. Accordingly, Applicant respectfully submits that the rejection of Claim 15 under 35 U.S.C. §102 as being anticipated by Grochowski is in error.

Claims 2 and 6 are dependent on patentably independent Claim 1, as discussed above, and those arguments are hereby incorporated regarding Claims 2 and 6. At least for this reason, Applicant respectfully submits that Claims 2 and 6 are allowable.

C. Group II: Rejection of Claims 3 and 16 Under 35 U.S.C. §102(e) as Being Anticipated by Grochowski

Claims 3 and 16 are dependent on patentably independent Claims 1 and 15, as discussed above, and those arguments are hereby incorporated regarding Claims 3 and 16. Additionally, Claims 3 and 16 are independently patentable as Grochowski fails to disclose estimating an amount of power used by a microprocessor based on (1) the count value associated with at least one activity, (2) current clock frequency and (3) operating voltage level of the microprocessor, as set forth in Claims 3 and 16.

In rejecting Claims 3 and 16, the Examiner asserts that Grochowski discloses estimating an amount of power used by a microprocessor based on (1) the count value associated with at

least one activity, (2) current clock frequency and (3) operating voltage level of the microprocessor, citing figure 4-5, column 2, lines 6-17 of Grochowski. However, these figures and passages referred to in Grochowski in no way teach or suggest estimating an amount of power used by a microprocessor based on (1) the count value associated with at least one activity, (2) current clock frequency and (3) operating voltage level of the microprocessor. Rather, Grochowski teaches a digital throttle that estimates a power consumption of a processor based on activity states of the processor's functional units. Since Grochowski fails to or suggest the limitations as recited in Claims 3 and 16, the rejection of Claims 3 and 16 are in error.

D. Group III: Rejection of Claims 8, 9, 10 and 13 Under 35 U.S.C. §102(e) as Being Anticipated by Grochowski

The Examiner rejects Claims 8, 9, 10 and 13 under 35 U.S.C. §102(e) as being anticipated by Grochowski. In rejecting Claim 8 under 35 U.S.C. §102 as being anticipated by Grochowski, the Examiner erred in concluding that Grochowski discloses estimating an amount of power used by a microprocessor based on information provided by a counter. Applicant respectfully submits that Grochowski does not disclose estimating an amount of power used by a microprocessor based on information provided by at least one counter, much less controlling at least one throttling mechanism incorporated in the microprocessor based on the estimated power usage, as recited in Claim 8. Accordingly, the rejection of Claim 8 under 35 U.S.C. §102 as being anticipated by Grochowski is in error.

Claims 9, 10 and 13 are dependent on patentably independent Claim 8, as discussed above, and those arguments are hereby incorporated regarding Claims 9, 10 and 13. At least for this reason, Applicant respectfully submits that Claims 9, 10 and 13 are allowable.

E. Group IV: Rejection of Claims 19, 20, 21, 24, 26 and 27 Under 35 U.S.C. §102(e) as Being Anticipated by Grochowski

The Examiner rejects Claims 19, 20, 21, 24, 26 and 27 under 35 U.S.C. §102(e) as being anticipated by Grochowski. In rejecting Claim 19 under 35 U.S.C. §102 as being anticipated by Grochowski, the Examiner erred in concluding that Grochowski discloses estimating an amount of power used by a microprocessor based on information provided by a counter. Applicant

respectfully submits that Grochowski does not disclose [1] receiving information provided by at least one counter, [2] estimating an amount of power used by a microprocessor based on information provided by at least one counter, and [3] controlling at least one throttling mechanism incorporated in the microprocessor based on the estimated power usage, as recited in Claim 19. Accordingly, the rejection of Claim 8 under 35 U.S.C. §102 as being anticipated by Grochowski is in error.

Claims 20, 21, 24, 26 and 27 are dependent on patentably independent Claim 19, as discussed above, and those arguments are hereby incorporated regarding Claims 20, 21, 24, 26 and 27. At least for this reason, Applicant respectfully submits that Claims 20, 21, 24, 26 and 27 are allowable.

F. Group V: Rejection of Claims 4, 11, 17 and 22 Under 35 U.S.C. §103(a) as Being Unpatentable over Grochowski in View of Kenny

Applicant incorporates its prior arguments with respect to the failure of Grochowski to anticipate Claims 1, 8, 15 and 19, from which Claims 4, 11, 17 and 22 depend. Applicant also notes that Grochowski fails to disclose estimating an amount of power used by a microprocessor by averaging the current estimated power usage value with a defined number of most recently estimated power usage values obtained during previous sampling time periods, as set forth in Claims 4, 11 and 22. Furthermore, Grochowski fails to disclose adjusting the estimated amount of power usage by applying recently estimated power usage values obtained during previous sampling time periods with the current estimated power usage value, as set forth in Claim 17. Therefore, the rejection of Claims 4, 11, 17 and 22 is erroneous.

G. Group VI: Rejection of Claims 5, 12, 18 and 23 Under 35 U.S.C. §102(e) as Being Anticipated by Grochowski

Applicant incorporates its prior arguments with respect to the failure of Grochowski to anticipate Claims 1, 8, 15 and 19, from which Claims 5, 12, 18 and 23 depend. Applicant further notes that Grochowski fails to disclose activating a throttling mechanism if the estimated power used by the microprocessor is greater than a defined threshold and deactivating the throttling mechanism if the estimated power used by the microprocessor is less than the threshold, as set

forth in Claims 5, 12, 18 and 23. Therefore, the rejection of Claims 5, 12, 18 and 23 is erroneous.

H. Group VII: Rejection of Claims 7, 14 and 25 Under 35 U.S.C. §102(e) as Being Anticipated by Grochowski

Applicant incorporates its prior arguments with respect to the failure of Grochowski to anticipate Claims 1, 8 and 19, from which Claims 7, 14 and 25 depend. Applicant further notes that Grochowski fails to disclose that one of the activities monitored is one of the following activities; (1) floating point operation, (2) cache memory access and (3) instruction decoding, as set forth in Claims 7, 14 and 25.

Furthermore, Applicant respectfully submits that the Examiner has not carried the burden the patent law imposes on the Examiner by failing to point out where the claimed features of Claims 7, 14 and 25 are found within Grochowski. It is not Applicants responsibility to show that a claim is patentable until the Examiner first makes out a prima facie case of unpatentability. The Examiner is obligated to examine every claim both independent and dependent. Here the Examiner has not met that obligation. Therefore, the rejection of Claims 7, 14 and 25 is erroneous.

IX. CONCLUSION AND RELIEF

Based on the foregoing, Applicant requests that the Board overturn the rejection of all pending claims and hold that all of the claims of the present application are allowable.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Dated: March 3, 2004

Walter T. Kim, Reg. No. 42,731

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CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Mail Stop Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 03, 2004

Marilyn Bass March 03, 2004

X. APPENDIX

The claims involved in this Appeal are as follows:

1. (Previously Presented) A microprocessor comprising:

at least one throttling mechanism; and

a thermal control subsystem to estimate an amount of power used by said microprocessor and to control said at least one throttling mechanism based on said estimated power usage, wherein the thermal control subsystem is in communication with at least one counter and the thermal control subsystem estimates the amount of power used by the microprocessor based on information provided by the at least one counter.

2. (Original) The microprocessor of claim 1, wherein the amount of power used by the microprocessor is estimated based on the number of occurrences of at least one activity performed in said microprocessor.

3. (Original) The microprocessor of claim 1, wherein thermal control subsystem includes a power usage monitoring unit which determines the number of occurrences of at least one activity performed by the microprocessor within a sampling time period and computes the estimated power usage based on (1) the count value associated with said at least one activity, (2) current clock frequency and (3) operating voltage level of the microprocessor

4. (Original) The microprocessor of claim 3, wherein the power usage monitoring unit estimates the amount of the power used by the microprocessor by averaging the current estimated power usage value with a defined number of most recently estimated power usage values obtained during previous sampling time periods.

5. (Original) The microprocessor of claim 1, wherein the thermal control subsystem further comprises a throttling control unit which compares said estimated amount of power used by the microprocessor against a threshold and activates the throttling mechanism if the estimated power used by the microprocessor is greater than said threshold or deactivates the throttling mechanism if the estimated power used by the microprocessor is less than said threshold.

6. (Original) The microprocessor of claim 1, wherein the throttling mechanism is activated in a deterministic manner by the thermal control subsystem.

7. (Original) The microprocessor of claim 2, wherein said at least one activity monitored by the thermal control subsystem comprises at least one of the following activities; (1) floating point operation, (2) cache memory access and (3) instruction decoding.

8. (Previously Presented) A method comprising:

receiving information provided by at least one counter;

estimating an amount of power used by a microprocessor based on the information provided by the at least one counter; and

controlling at least one throttling mechanism incorporated in the microprocessor based on said estimated power usage.

9. (Original) The method of claim 8, wherein the amount of power used by the microprocessor is estimated based on the number of occurrences of at least one activity performed in the microprocessor.

10. (Original) The method of claim 8, wherein the estimating the amount of power used by the microprocessor further comprises:

counting the number of occurrences of at least one activity performed by the microprocessor within a sampling time period; and

adjusting the number of occurrences of said at least one activity according to current operating frequency and voltage level of the microprocessor.

11. (Original) The method of claim 10, wherein the estimating the amount of the power used by the microprocessor further comprises averaging the current estimated power usage value with a defined number of most recently estimated power usage values obtained during previous sampling time periods.

12. (Original) The method of claim 8, further comprising:

comparing said estimated amount of power used by the microprocessor against a threshold;

activating said at least one throttling mechanism if said estimated power used by the microprocessor is greater than said threshold; and

deactivating said at least one throttling mechanism if said estimated power used by the microprocessor is less than said threshold.

13. (Original) The method of claim 8, wherein the throttling mechanism is activated in a deterministic manner.

14. (Original) The method of claim 10, wherein said at least one activity monitored is selected from the following activities; (1) floating point operation, (2) cache memory access and (3) instruction decoding.

15. (Previously Presented) A thermal control system comprising:

a power usage estimator coupled to at least one counter, the power usage estimator to estimate an amount of power used by a microprocessor based on information provided by the at least one counter; and

a throttling control unit to control at least one throttling mechanism incorporated in the microprocessor based on the estimated amount of power used by the microprocessor.

16. (Original) The thermal control system of claim 15, wherein said power usage estimator estimates the amount of power used by the microprocessor based on (1) the number of occurrences of at least one activity, (2) current clock frequency and (3) operating voltage level of the microprocessor.

17. (Original) The thermal control system of claim 15, further comprising a filter to adjust the estimated amount of power usage by applying recently estimated power usage values obtained during previous sampling time periods with the current estimated power usage value.

18. (Original) The thermal control system of claim 15, wherein said throttling control unit compares said estimated amount of power used by the microprocessor against a threshold and activates the throttling mechanism if the estimated power used by the microprocessor is greater than said threshold or deactivates the throttling mechanism if the estimated power used by the microprocessor is less than said threshold.

19. (Previously Presented) A machine-readable medium that provides instructions, which when executed by a microprocessor cause said microprocessor to perform operations comprising:

receiving information provided by at least one counter;

estimating an amount of power used by a microprocessor based on the information provided by the at least one counter; and

controlling at least one throttling mechanism incorporated in the microprocessor based on said estimated power usage.

20. (Original) The machine-readable medium of claim 19, wherein the amount of power used by the microprocessor is estimated based on the number of occurrences of at least one activity performed in the microprocessor.

21. (Original) The machine-readable medium of claim 19, wherein the operation of estimating the amount of power used by the microprocessor further comprises reading count data representing the number of occurrences of at least one activity performed by the microprocessor within a sampling time period and adjusting the number of occurrences of said at least one activity according to current operating frequency and voltage level of the microprocessor.

22. (Original) The machine-readable medium of claim 21, wherein the operation of estimating the amount of the power used by the microprocessor further comprises averaging the current estimated power usage value with a defined number of most recently estimated power usage values obtained during previous sampling time periods.

23. (Original) The machine-readable medium of claim 19, wherein the operations further comprises:

comparing said estimated amount of power used by the microprocessor against a threshold;

activating said at least one throttling mechanism if said estimated power used by the microprocessor is greater than said threshold; and

deactivating said at least one throttling mechanism if said estimated power used by the microprocessor is less than said threshold.

24. (Original) The machine-readable medium of claim 19, wherein the throttling mechanism is activated in a deterministic manner.

25. (Original) The machine-readable medium of claim 21, wherein said at least one activity monitored is selected from the following activities; (1) floating point operation, (2) cache memory access and (3) instruction decoding.

26. (Previously Presented) The microprocessor of claim 1, wherein the at least one counter is implemented as a register in a hardware component.

27. (Previously Presented) The microprocessor of claim 1, wherein the at least one counter is implemented as a variable in software code.